Amendments to the Drawings begin on page 11 of this paper and include both an attached replacement sheet and an annotated sheet showing changes.

Remarks/Arguments begin on page 12 of this paper.

Amendments to the Drawings:

The attached sheet indicates changes to Fig. 1. This sheet replaces the previously submitted replacement sheet Fig. 1. The duplication of "110d" has been corrected.

Attachment: Replacement Sheet
Annotated Sheet Showing Changes

REMARKS

In view of both the amendments presented above and the following discussion, the Applicant submits that none of the claims now pending in the application is anticipated under the provisions of 35 USC § 102. Thus, the Applicant believes that all of these claims are now in allowable form.

If, however, the Examiner believes that there are any unresolved issues requiring adverse action in any of the claims now pending in the application, the Examiner should telephone Mr. Peter L. Michaelson, Esq. at (732) 530-6671 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Specification amendments

Various amendments have been made to the specification to correct minor inadvertent errors that remained in the specification.

Drawings

The Examiner objected to the Applicant's substitute drawing sheet for FIG. 1, filed with the immediately prior amendment mailed April 15, 2005. Specifically, the Examiner stated that the reference numeral "110d" was duplicated.

In response, the Applicant proposes to change the reference numeral for the connections between master 115c and slave 120c from "110d" to --110c--. To facilitate this

correction, the Applicant has enclosed a red-lined drawing sheet showing his proposed correction and a suitably corrected replacement drawing sheet. The Applicant now solicits the Examiner's approval of this change.

Status of Claims

Claims 1, 4, 5, 8, 11, 14, 19, 20, 23, 25 and 27-30 have now been cancelled and replaced by new claims 31-41. The new claims more precisely define the present invention than those now cancelled.

Rejections under 35 USC § 102

A. Rakib et al patent

The Examiner has rejected claims 1, 4, 5, 8, 11, 14, 19, 20, 23, 25 and 27-30 under the provisions of 35 USC § 102(e) as being anticipated by the teachings in the Rakib et al patent (United States patent 6,307,868 issued to Selim S. Rakib et al on October 23, 2001). Inasmuch as all these claims have now been cancelled, this rejection is moot. Nevertheless, to expedite prosecution, this rejection will be discussed in the context of new claims 31-41 and principally new independent claim 38. In that context, this rejection is respectfully traversed.

Specifically, the Examiner believes that each limitation of claim 1, as it stood prior to this amendment, is identically disclosed in the Rakib et al patent. In that regard, the Examiner opines that "the first controllable delay element" is collectively taught in block 65 in

Figure 1, and in col. 16, lines 5-29; and the "decision processor" is collectively taught in block 65 in Figure 1; col. 16, lines 5-29; Figure 6, col. 22, lines 8-26; and blocks 1512 and 467 in Figure 28.

As the Examiner will soon appreciate and with respect to claim 38, the recitations of a "metric processor" and the "decision processor", as they appear in this claim are not disclosed, taught or even suggested in the Rakib et al patent.

The Rakib et al patent discloses a system for bi-directional digital communication in which the system employs multiple channels with a master and a corresponding slave situated on opposite ends of each such channel. Generally speaking, so does the Applicant's inventive system.

As discussed in col. 1, line 45 et seq and col. 3, line 66 et seq of that patent, the patentee states that phase locked loops (PLLs) and continuous tracking loops, when used in a bi-directional digital data communications system, are not always reliable and add complication and expense to receivers. Consequently, this patent addresses the problem as to how to eliminate as many continuous tracking loops and PLLs as possible from a central unit (CU) receiver (or receiver in any unit having a transmitter than transmits the master clock and master carrier signals).

In essence and to the extent relevant to the present invention, this patent expressly teaches, in col. 3, line 57 et seq, the broad concept of having a local clock in

a remote (RU) synchronized to a master clock in the central unit and using that local clock, at the remote unit receiver, as a clock for a remote unit transmitter:

> "This technique is similar to the aspect of the invention involving having the remote unit local clock synchronized to the central unit master clock and using that local clock at the remote unit receiver for the remote unit transmitter."

Further and of critical interest, this patent also teaches the concept of adjusting the phase of the central unit master clock to synchronize it to the phase of the received clock from the remote unit transmitter and then using the resulting adjusted master clock signal as the clock signal from the central unit receiver. In that regard, the patent expressly states in col. 3, line 61 et seq:

> "It is also similar to the aspect of the invention of using the central unit master clock, after adjustment in phase to synchronize it to the phase of the received clock from the remote unit transmitter, as the clock signal from the central unit receiver."

As stated in col. 5, line 26 et seq, this adjustment is performed in the central unit receiver:

> "The central unit receiver can use any type of detector that is compatible with the modulation scheme used by the remote unit transmitter. ... The only requirement on this circuit is that it be able to occasionally or periodically detect any phase differential between the central unit master carrier and the carrier used to transmit by the remote unit transmitter and detect any phase difference between the central unit master clock and the clock information used to transmit the received data. These phase differences are used by the *central unit receiver to*

> *occasionally or periodically adjust the phase of the master clock and master carrier* to match the phases of the carrier and clock signals used by the remote unit transmitter as received at the central unit receiver." [emphasis added]

See, also, col. 16, lines 55 et seq which detail the functions of the phase detect and adjust circuit 32 within the central unit.

Further, this patent also teaches incorporating a fixed delay, Td, into a data stream to be transmitted by each remote unit. As discussed in col. 16, lines 5-29, this delay, in contrast to the Examiner's apparent belief that it would generate the slave clock transmit signal by delaying a slave clock receive signal, merely compensates the remote unit for its physical distance from the central unit and thus aids the remote unit in achieving frame synchronization with the central unit. These lines, in pertinent part, state:

> "The upstream data output from the encoder 60 on line 64 is received by an adjustable delay circuit 65 which receives an adjustable delay value Td. This circuit is used when the system of FIG. 1 requires frame synchronization and the remote units are at differing distances from the central units. ... *The value of Td is adjusted for each remote unit based upon its physical distance from the central unit so as to achieve frame synchronization.*" [emphasis added]

Inasmuch as the system taught by the Rakib et al patent is synchronous (specifically synchronous code division multiple access -- SCDMA), all signals from the remote units must be received at the central unit with

exactly aligned frame boundaries. In that regard, col. 20, line 29 et states:

> "The process of synchronization is the process wherein each RU has a variable delay in its transmitter set using feedback from the CU on one of the management and control channels such that the transmitted frame from each RU arrives at the CU with its frame boundaries exactly aligned with the frame boundaries of the frames from the other RUs."

Since the SCDMA system relies on carrying its signal over a physical media, then on a hot summer day, this media, as indicated in col. 21, line 45 et seq, can thermally expand. Such expansion can cause frame misalignment. As discussed in col. 22, line 9 et seq, when such misalignment occurs, the RU will change its delay on a trial and error basis until frame alignment is restored. Unfortunately, if the delay value, Td, has been incremented a number of times, then the RU may be aligned with the start of a wrong frame (e.g., one which is one frame later than desired). To remedy this, the Rakib et al patent teaches, as discussed in col. 22, line 27 et seq, the concept of imposing a delay at the central unit in transmitting an alignment triggering signal (Barker code) and then reducing this delay as needed to achieve proper frame synchronization with the remote unit. As stated in col. 23, line 20 et seq, once the CU has reduced its delay, the RU will continue to change its delay time, Td, on a trial and error basis in an attempt to attain frame alignment.

In that regard, this process is summarized in col. 24, line 33 et seq with reference to FIGs. 5A-5C:

> "[T]here is shown a flowchart for the general alignment/ranging process which is used in training all RUs to set their transmit frame timing delays Td properly such that each frame transmitted by an RU will arrive at the CU at the same time as all other frames transmitted from other RUs despite differing propagation times."

The Applicant's inventive approach, while in a very broad sense may appear to be facially similar to that taught by the Rakib et al patent, in actuality, the former strikingly differs from the latter.

In particular, the present invention is not directed to the problem of maintaining frame alignment but rather to reducing the affect, in a near-end receiver in a master, of distortion caused by near end cross-talk (NEXT) and echo contained within a relatively short burst on incoming signals from a far-end slave to that receiver. This distortion results from an A/D converter, which in the master receiver samples the incoming signal, taking a sample during a time when the NEXT/echo burst has a relatively high amplitude.

In accordance with the inventive teachings, distortion is significantly reduced by adjusting the sample time Ts in the master receiver and, also and importantly, by selectively and controllably delaying the transmit clock in the slave. As to the latter, a metric processor (270 as shown in FIG. 1 of the present application) in the master measures incoming sample values of a signal received from a

slave against allowed sample values for that signal to determine the amount of ambiguity between the two (i.e., where a sample is taken within an eye pattern as shown in FIG. 4). Specifically, FIG. 4 shows an eye pattern in which NEXT/echo burst occurs in the incoming signal. The NEXT/echo burst (pulse) typically appears as a relatively high amplitude portion "b" followed by a relatively low amplitude portion "c". Given that a high amplitude portion "b" is typically shorter in duration than the separation distance "a" in the eye diagram, then by delaying the slave transmit clock to occur within low amplitude portion "c", the incoming sample taken during portion "c" will be far less distorted than that taken during portion "b". Decision processor 285, in response to the data (metric signal) provided by the metric processor, determines the proper amount of delay and, through near-end transmitter 130, issues a command to the slave. In response to this command, receiver 236, acting through controller 260, sets the delay provided by element 232 in the slave to delay the slave transmit clock accordingly. Alternatively, the decision processor can simply set this delay to different successive values until an optimum delay value is found. The optimum value of delay, which minimizes the effects of NEXT/echo, occurs when the metric signal is maximized. See, e.g., page 11, line 11 et seq of the present specification.

Hence, through the present invention, the master, based on measurements of the incoming received signal from the slave, calculates the proper amount of delay that the SLAVE should impart to its local transmit clock and then instructs the slave to provide that delay.

Nowhere does the Rakib et al patent contain any teachings regarding how to reduce the effects of NEXT/echo let alone, as the present Applicant teaches, by having the master determine the amount of delay that a slave should impart to its slave transmit clock and then instruct that slave to set that delay accordingly. All the Rakib et al patent teaches is that the slave data output (the Rakib et al patent refers to a slave as a remote Unit -- RU) to provide frame synchronization among all RU's such that all frames from all the RU's arrive at the CU (which with the same exact alignment. Even if one were to inferentially view the teachings in the Rakib et al patent as applicable to reducing the effects of NEXT/echo, its teachings fall far short of the present invention. In that regard, there are absolutely no teachings in this patent, let alone any circuitry or process steps, through which the CU calculates the amount of delay that each RU is to be provide to its data output or local transmit clock (changes to the latter being taught by the present invention) and then instructs that RU to provide. As discussed in col. 23, line 20 et seq in the Rakib et al patent and referenced above, each RU simply changes its delay on a trial and error basis, apparently independently of any delay adjustments being made by the master to its master clock and master carrier.

Hence, the Applicant submits that his present invention is not disclosed, taught or suggested -- even implicitly, by the teachings of the Rakib et al patent.

New independent claim 38 contains suitable recitations directed to the distinguishing aspects of the Applicant's present invention. In particular, this claim

recites as follows with those recitations shown in a bolded typeface:

> "Apparatus for a bi-directional communication link having a plurality of channels with a master and a slave at respective ends of each one of the channels so as to define respective pluralities of masters and slaves, the master issuing a Master Tx clock, the slave constructing both a Slave Rx clock frequency-locked to the Master Tx clock and a Slave Tx clock frequency-locked to the Slave Rx clock, said apparatus comprising:
>
> **a metric processor, situated within said master, which produces a metric signal reflective of amplitude differences between a signal received by the master from a corresponding one of the slaves and allowed amplitude levels of the received signal; and**
>
> **a decision processor, connected to the master and responsive to the metric processor, for changing phase of the Slave Tx clock relative to the Slave Rx clock in the corresponding one of the slaves in order to maximize the metric signal produced by the metric processor and thereby reduce distortion caused by near end cross-talk and echo in signals received over the channel by a receiver in the master and thus facilitate clock and data recovery by the receiver.**" [emphasis added]

Similar recitations appear in the other independent claim, now pending in the application, namely claim 31.

Accordingly, the Applicant submits that neither independent claim 31 nor claim 38 is anticipated by the teachings in the Rakib et al patent. Hence, both of these claims are patentable under the provisions of 35 USC § 102.

Each of the remaining claims, i.e., dependent claims 32-37 and 39-41, depends from independent claims 31 and 38, respectively, and recites further distinguishing

features of the present invention. Accordingly, the Applicant submits that each of these dependent claims is patentable over the teachings of the Rakib et al patent for the same reasons set forth above. Therefore, each of these dependent claims is patentable under the provisions of 35 USC § 102.

B. Trans patent

The Examiner has also rejected claims 1, 4, 5, 8, 11, 14, 19, 20, 23, 25 and 27-30 under the provisions of 35 USC § 102(e) as being anticipated by the teachings in the Trans patent (United States patent 6,377,640 issued to Francois Trans on April 23, 2002). Since all these claims have now been cancelled, this rejection is also moot. Nevertheless, to expedite prosecution, this rejection will be discussed in the context of new claims 31-41 and principally new independent claim 38. In that context, this rejection is also respectfully traversed.

Specifically, the Examiner believes that each limitation of claim 1, as it stood prior to this amendment, is identically disclosed in the Trans patent. In that regard, the Examiner opines, that "the first controllable delay element" is collectively taught in Figure 34, and in col. 64, line 32; and the "decision processor" is collectively taught in block M212 in Figure 5a, and in col. 16, lines 37-38.

As the Examiner will soon appreciate and with respect to claim 38 -- and as was the case with the Rakib et al patent, the recitations of a "metric processor" and the

"decision processor", as they appear in this claim are not disclosed, taught or even suggested in the Trans patent either.

For the sake of brevity, the Applicant will not repeat his discussion of the present invention, but instead will merely direct the Examiner's attention to that discussion in the preceding section above.

The Trans patent discloses a synchronous digital data transmission system for a 2 GBit/second (2000 Base T) network and specifically an approach for use within that system for synchronizing nodes on such a network using a clock transfer system. The goal is to reduce distortion, arising from data lying outside of defined phase and frequency ranges, that would otherwise cause errors in data signaling and, in turn, reduce channel bandwidth and data throughout. As discussed in col. 7, line 49 et seq of this patent, the approach involves measuring a channel, coding a new signal that will be carried over that channel using precise control over that signal's frequency and phase, and adjusting the signal to eliminate distortion that would otherwise arise at very high data transmission speeds over the channel. Col. 8, line 3 et seq states that this approach is realized through a clock transfer system through which synchronous phase and frequency information transfers from one network node to another and proliferates throughout an entire network. In that regard, a reference source generates a given clock signal from which appropriately corrected frequency and phase information is transmitted across the entire network. See also col. 10, lines 3 et seq. The goal being to ensure that every cock signal in

each node arrives within a predicted phase interval. See, col. 24, line 32 et seq.

Specifically and as indicated on col. 11, line 8 et seq, the Trans system involves training each network node. This entails determining, for that network node (station), phase and frequency offsets of received data from that node with respect to the reference source (clock). Those offsets are then sent back to the that node to tune its local oscillator, with this process repeating itself until the local reference received from that station falls within designated tolerances. Once the frequency of the local oscillator is set, then, as indicated through block M212 shown in FIG. 5a and discussed in col. 16, lines 37-38, the fine tuning of the phase occurs through which the phase of that oscillator is appropriately set.

The Examiner should note a <u>fundamental distinction</u> between the approach taught by the Trans patent and that taught by the present Applicant. In the former, the local oscillator in each station, which serves as a local reference for that station, is set through receipt of frequency and phase information. The Applicant's inventive system calculates, in a master, an appropriate delay value for use in a corresponding slave, through which the slave receive clock itself is modified to yield the slave transmit clock. The slave receive clock is recovered from the signal received in the slave and transmitted by the master. Once the delay value is determined, the master instructs the slave to delay its slave receive clock by that amount to yield the slave transmit clock. The present inventive system does <u>not</u> change the slave receive clock, as that is a

reference clock used throughout the slave -- in contrast to the system taught by the Trans patent which apparently changes both the frequency and phase of that clock and as a result any other local clock that is generated from it.

Furthermore, to determine the appropriate offsets, the Trans patent teaches the notion of computing a so-called error vector magnitude (EVM). The EVM, with respect to amplitude and as discussed in col. 31, line 42 et seq, reflects the "average voltage level of all the symbols (a value closest to the average signal level) or by the voltage of the outermost (highest voltage) four symbols". In contrast, the metric signal produced by the metric processor in the Applicant's inventive system reflects amplitude differences in the incoming sampled signal between its actual amplitude values and its allowed amplitude values -- not average values or highest actual values.

The teachings of the Trans patent, like the Rakib et al patent, simply stop short of the present invention and contain no suggestions that would motivate one of skill in the art to modify those teachings to yield the Applicant's inventive approach.

Hence, the Applicant submits that his present invention is not disclosed, taught or suggested -- even implicitly, by the teachings of the Trans patent.

As discussed and delineated above, each of independent claims 31 and 38 contains suitable recitations directed to the distinguishing aspects of the Applicant's present invention.

Accordingly, the Applicant submits that neither independent claim 31 nor claim 38 is anticipated by the teachings in the Trans patent. Hence, both of these claims are patentable under the provisions of 35 USC § 102.

Each of the remaining claims, i.e., dependent claims 32-37 and 39-41, depends from independent claims 31 and 38, respectively, and recites further distinguishing features of the present invention. Accordingly, the Applicant submits that each of these dependent claims is patentable over the teachings of the Trans patent for the same reasons set forth above. Therefore, each of these dependent claims is patentable under the provisions of 35 USC § 102.

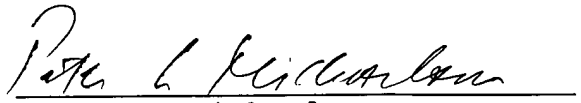
Conclusion

Thus, the Applicant submits that none of the claims, presently in the application, is anticipated under the provisions of 35 USC § 102.

Consequently, the Applicant believes that all these claims are presently in condition for allowance.

Respectfully submitted,

October 3, 2005



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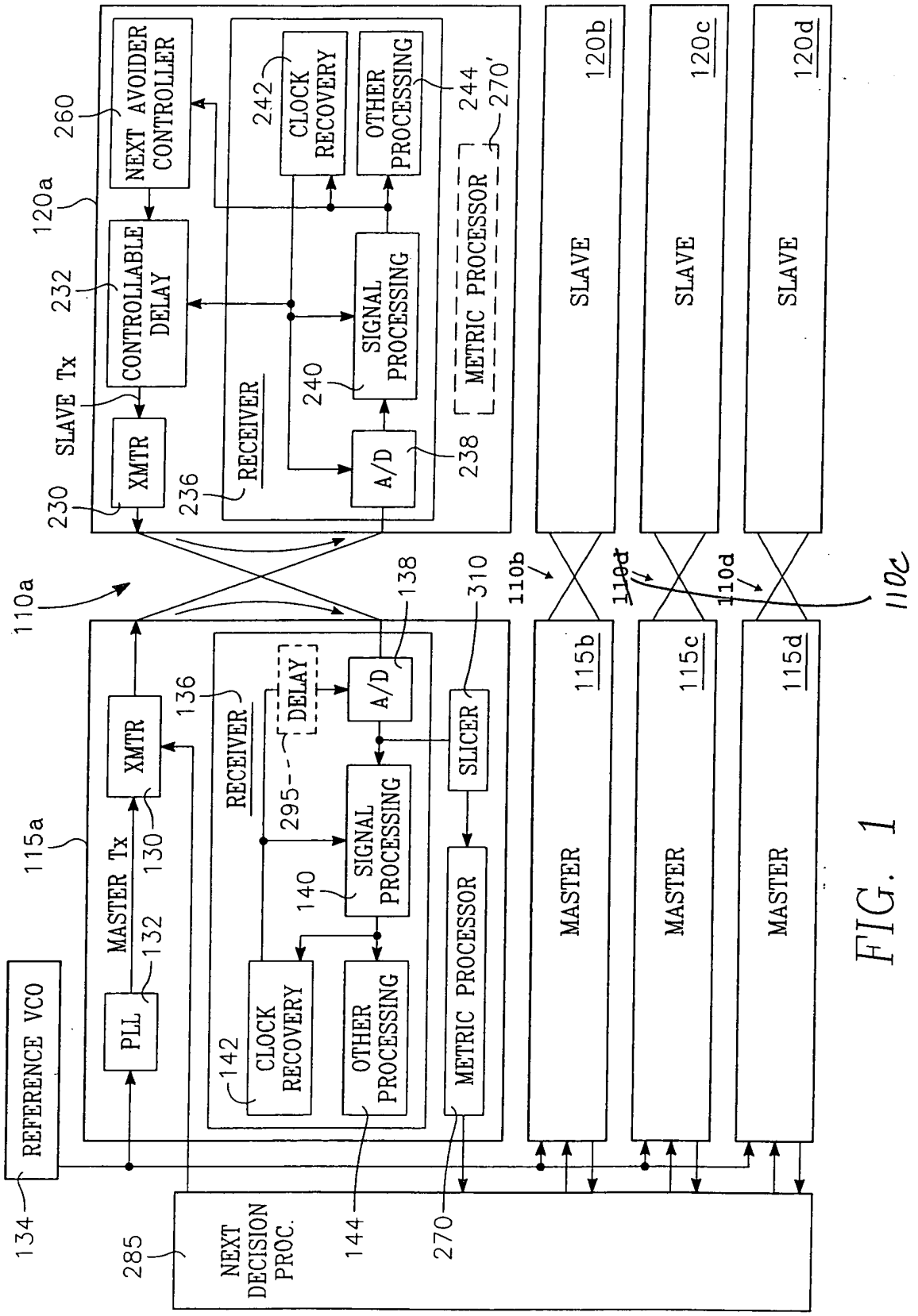

FIG. 1